C-Band 6-Bit GaAs Monolithic Phase Shifter

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Abstract—**Design, fabrication, and performance of a 6-bit GaAs monolithic phase shifter for use in the 5–6-GHz frequency range are described. The chip includes an analog control bit (0–11°) for phase correction in a closed-loop configuration and five digitally controlled phase bits. A ±1° phase variation was achieved for the 11.25°, 22.5°, and 45° bits while for the 90° and 180° bits the phase variation was ±6° over 5 to 6 GHz. The return loss was better than 15 dB and insertion-loss flatness was within ±1 dB over this frequency band. The phase error over a temperature range of 25–80°C and the 5–6-GHz frequency band was less than ±0.5°, ±1°, ±1°, ±2°, and ±2° for the 11.25°, 22.5°, 45°, 90°, and 180° bits, respectively, with a maximum of .8-dB insertion-loss variation.**

I. Introduction

PHASED-ARRAY RADARS using elemental tranceivers will rely on monolithic programmable microwave integrated circuits to achieve minimum size, weight, power consumption, and cost. For beam steering, programmable reciprocal-phase shifters will be used to adaptively adjust transceiver phase in both the transmit and receive mode. To achieve maximum effectiveness, the sidelobes of the beams must be maintained very low. This requirement imposes severe specifications on the programmable phase shifter accuracy.

Most large practical systems use 4-bit phase shifters as a compromise between the cost, size, insertion loss, and the incremental improvement in system performance when more phase bits are used. Monolithic microwave integrated circuit 4-bit phase shifters [1]–[4] and 5-bit phase shifters [5] have been reported in the literature. However, for applications which demand very low sidelobe levels with a fewer number of array elements, up to 8-bit phase shifters have been used.

This paper reports on the design, fabrication, and test results of a GaAs monolithic phase shifter which contains a 5-bit digital circuit along with an analog circuit bit for fine phase tuning. The analog may be used as a sixth digital bit.

II. Characterization of FET Switch

Although the FET itself is a three-terminal device, the switching mechanism takes place between the drain and the source with the control voltage applied to the gate. In this configuration, the FET behaves as a passive element, and only dc power consumption is due to gate leakage current. FET switches with different gate peripheries were characterized theoretically as well as by measuring *S*-parameters and dc resistances. An accurate model for the FET switch consisting of a seven-element *RLC* network was obtained. The CALMA layout for a typical FET switch with dimensions is shown in Fig. 1 while its equivalent *RLC* model is shown in Fig. 2. For various gate peripheries, *RLC* values are given in Table I. These values depend on the channel geometry, active layer doping, pinchoff voltage, and n^+ doping.

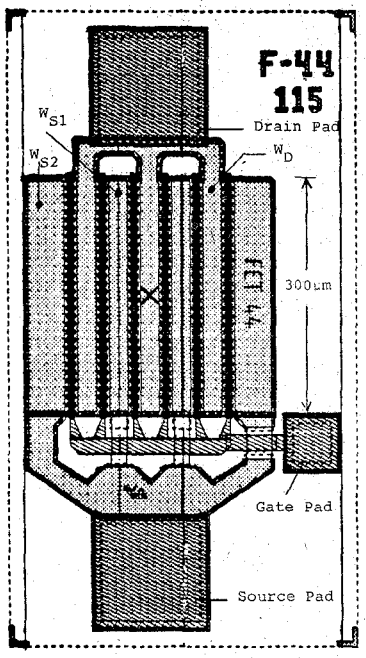

Fig. 1. CALMA layout for an 1800-μm gate periphery FET switch ($W_{S1} = W_D = 30$ μm and $W_{S2} = 70$ μm).

The gate in this FET switch configuration is not isolated from the drain as the drain and source terminals are at ground potential. As a consequence of this, the RF impedance of the gate bias circuit affects the drain–source impedance of the FET switch [1]. In the present design, the gate is biased through a 5-k Ω resistor which provides sufficient isolation between the gate terminal and the bias supply.

III. 6-Bit Circuit Topology

The 6-bit phase shifter circuit consists of five digital bits (11.25°, 22.5°, 45°, 90°, and 180°) and an analog 0–11° bit cascaded in a linear arrangement, shown schematically in Fig. 3. The variable bit and 11.25°, 22.5°, and 45° bits are loaded-line type and the 90° and 180° bits are reflection-type phase shifter circuits. The variable bit consists of

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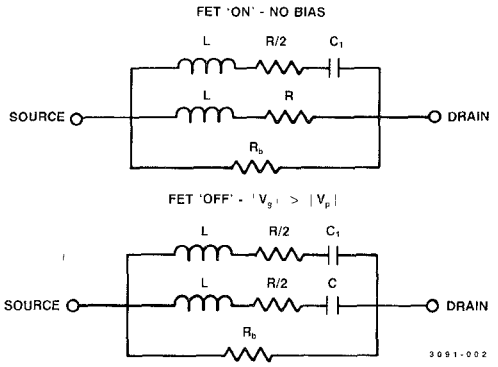

Fig. 2. FET switch equivalent circuits in ON and OFF states (V_g is the gate bias voltage and V_p is the pinchoff voltage of the FET).

TABLE I
FET SWITCH PARAMETERS FOR 1-μm GATE LENGTH

FET Size	Element Values				
(μm)	R (Ohm)	R_b (Ohm)	L (nh)	C (pF)	C_1 (pF)
1200	5.5	3000	.16	.17	.19
1800	4.2	2250	.13	.255	.285
2400	2.8	1500	.09	.34	.38

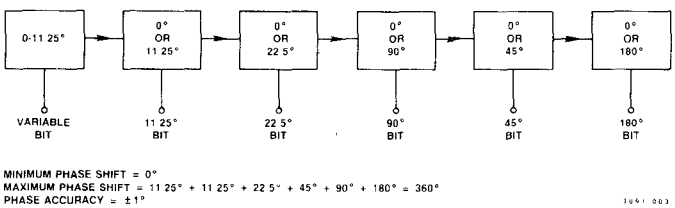

Fig. 3. Schematic of the 6-bit phase shifter.

an 11.25° bit that uses the FET's in a variable impedance mode to adjust the phase shift from 0 to 11 degrees. The 45° bit is positioned between the 90° and 180° bits to maintain the optimum overall VSWR over the designed bandwidth.

IV. Circuit Design

Each phase bit was designed and optimized individually to have at least 15-dB return loss so that modeling the entire phase shifter would not be necessary. The CAD tools used for designing these circuits were in-house computer program and TOUCHSTONE (EEsof). The final design for each bit includes the transmission-line losses and circuit and layout discontinuities. The design of loaded-line- and reflection-type phase bits is described below.

V. Loaded-Line Phase Shifters

The principle of operation of loaded line phase shifters using either FET switches or p-i-n diode switches is the same. The theory of operation of loaded line p-i-n diode digital phase shifters is well described in the literature

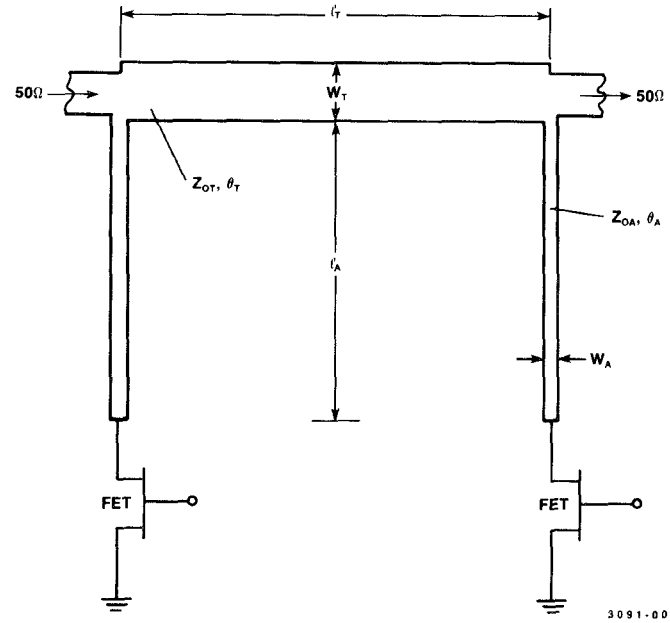

Fig 4. Schematic for 11.25°, 22.5°, and 45° loaded-line phase bits.

[6]–[14]. Loaded-line phase shifters consist of approximately quarter-wave long transmission lines of about 50 Ω, loaded at both ends with high-impedance stubs terminated with the FET switches. Periodic loading of a transmission line with lumped reactances is a well-known technique for varying the transmission characteristics of the line. Loaded-line phase shifters are based on this principle. The amount of phase shift provided by a pair of susceptances shunting a line is approximately equal to the difference of the normalized susceptances (with respect to transmission-line characteristic impedance) from the 'on' to 'off' states of the FET. In this configuration, reflections from any symmetric pair of small shunt susceptances spaced a quarter-wavelength apart will mutually cancel. Smaller phase shifts are best realized using the loaded-line phase type due to their lower insertion loss, higher power handling capability, and small size. The return loss of a loaded-line phase shifter, other than at center frequency, gets progressively worse as the required phase shift value increases. The FET size for each bit was optimized for best VSWR and lowest insertion loss, resulting in three different FET peripheries in the circuit: 1200 μm, 1800 μm, and 2400 μm. These large FET's also give rise to higher average power handling capability due to large current capabilities. For higher peak power handling capability, FET's with larger breakdown voltages are required. The schematic for these circuits is given in Fig. 4. Design details are given in Table II. The specifications for 11.25°, 22.5°, and 45° bits are summarized in Table III.

VI. Reflection-Type Phase Shifter

Reflection-type phase shifters are based on the principle of reflection of a signal from the termination of a transmission line. The theory of operation of hybrid coupled reflection-type digital phase shifters using p-i-n diodes have been studied by various researchers [15]–[19], and the same

TABLE II
ELECTRICAL AND PHYSICAL PARAMETERS FOR LOADED-LINE PHASE BITS.

Bit Size (Degree)	Z_{0T} (Ω)	θ_T (Deg.)	W_T (μm)	ℓ_T (μm)	Z_{0A} (Ω)	θ_A (Deg.)	W_A (μm)	ℓ_A (μm)	FET Size (μm)
11.25	50.5	88.5	88	4674	100	112.5	8	6030	2400
22.5	45	85	114	4450	90	113.5	14	6325	1200
45.0	48	78.3	100	4115	56.5	116.5	66	6223	1800

TABLE III
LOADED-LINE PHASE BITS SPECIFICATIONS.

Performance	Variable Bit (0-11°)	11.25° Bit	22.5° Bit	45° Bit
Frequency Range (GHz)	5-6	5-6	5-6	5-6
Phase Error (Degrees)	±1°	±2°	±2°	±2°
Max. Insertion Loss (dB)	1	1	1.2	2.0
Input & Output Return Loss (dB)	>20	>20	>15	>12

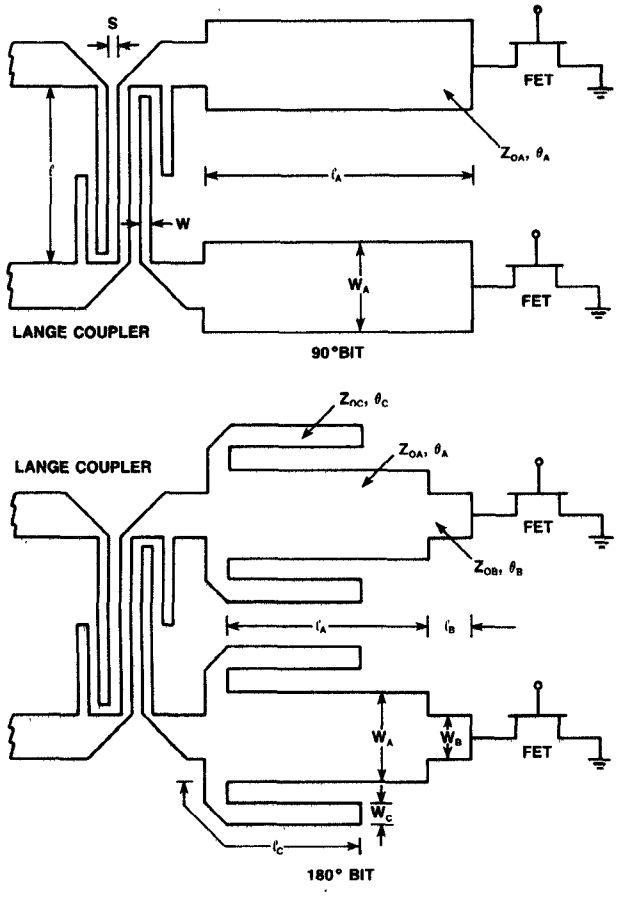

Fig. 5. Schematic for 90° and 180° reflection-type phase bits.

theory applies to FET switches. A transmission line terminated by a FET switch (switching between 'on' and 'off' states) acts as a one-port reflection phase bit. To make it a useful phase shifter circuit, the incident and reflection signals must be separated. This separation of signal can be obtained by using a 3-dB hybrid.

The required phase shift is obtained by adjusting the line parameters between the hybrid ports and the FET switches.

TABLE IV
ELECTRICAL AND PHYSICAL PARAMETERS FOR REFLECTION-TYPE PHASE BITS

90° Bit		180° Bit	
Z_{0A}	= 44 Ω	Z_{0A}	= 33.2 Ω
θ_A	= 14.6°	θ_A	= 20°
W_A	= 120 μm	W_A	= 204 μm
ℓ_A	= 762 μm	ℓ_A	= 1016 μm
FET Size	= 2400 μm	Z_{0B}	= 77.5 Ω
		θ_B	= 19.5°
		W_B	= 26 μm
		ℓ_B	= 1067 μm
		Z_{0C}	= 70 Ω
		θ_C	= 30.4°
		W_C	= 36 μm
		ℓ_C	= 1650 μm
		FET Size	= 2400 μm

In the present circuits (90° and 180° bits), Lange couplers are used. The 90° and 180° bit circuit parameters and FET sizes were optimized for best VSWR and lowest insertion loss. Schematics for these circuits are given in Fig. 5. Design details are given in Table IV. The specifications for 90° and 180° bits are summarized in Table V. For the Lange coupler, $W = S = 12$ μm and $l = 4966$ μm.

VII. 6-Bit Phase Shifter Layout

The CALMA layout of the phase-shifter circuit is shown in Fig. 6. In order to reduce the overall chip length, the transmission lines are folded with sufficient line spacing to avoid interline coupling. The Lange couplers are folded to keep the 90° and 180° bit sizes similar to other bit sizes. All the bits were designed to interface to 50 Ω, so that individual testing of the bits might be easily accomplished. The linear arrangement allows dicing the individual bits for comparative measurements. The switching FET's are arranged along the edge to accommodate the control leads from the chip and to allow short ribbon ground connections to the FET source pads. The next iteration will

TABLE V
REFLECTION-TYPE PHASE BITS SPECIFICATIONS.

Performance	90° Bit	180° Bit
Frequency Range (GHz)	5-6	5-6
Phase Error (Degrees)	±5	±5
Max. Insertion Loss (dB)	2	2
Input & Output Return Loss (dB)	>14	>14

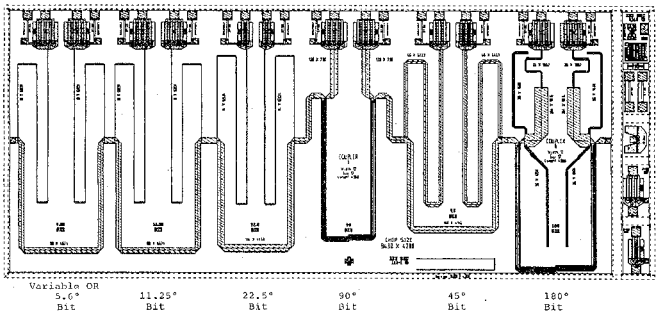

Fig. 6. Composite CALMA layout for the 5–6-GHz 6-bit phase shifter circuit.

TABLE VI
6-BIT PHASE SHIFTER CHIP STATISTICS.

Chip Size: 9.43 x 4.2 x .125 mm
Number of FETs: 12
FET Gate Length: 1 μm
Total Gate Periphery: 25.2 mm
Total Mesa Resistors (5kΩ each): 12
Total Air Bridges: 50
Lange Couplers: 2

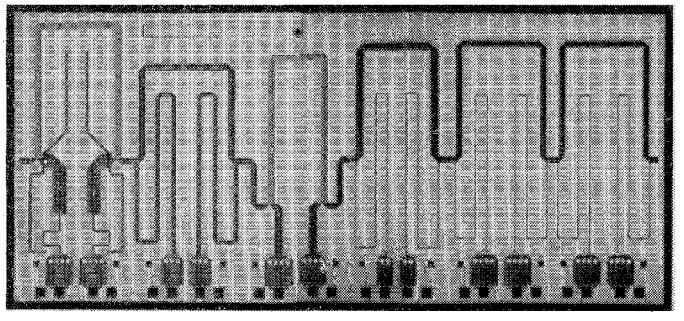

Fig. 7. Photograph of the 6-bit phase shifter.

include VIA holes for more uniform source grounding. All FET bias connections are mde through resistors for RF isolation and are individually brought out to pads. The circuits are completely dc coupled. No capacitors are used on the chip. The 6-bit phase shifter chip statistics are summarized in Table VI.

VIII. FABRICATION

The circuits were manufactured using the standard ITT Gallium Arsenide Technology Center process for ion-implanted GaAs. The active layer has doping $n = 2 \times 10^{17}$ cm^{-3} and thickness $t \cong 0.2$ μm. The process includes

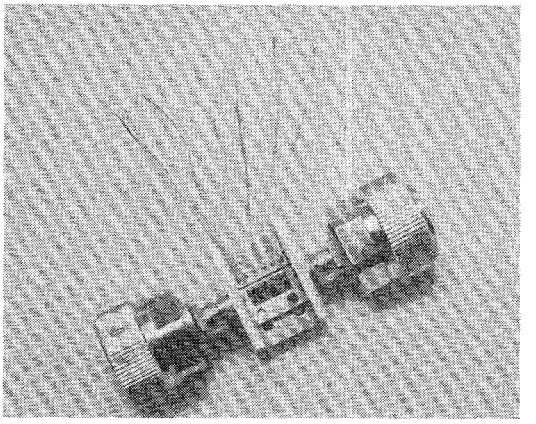

Fig. 8. 6-bit phase shifter chip in test fixture.

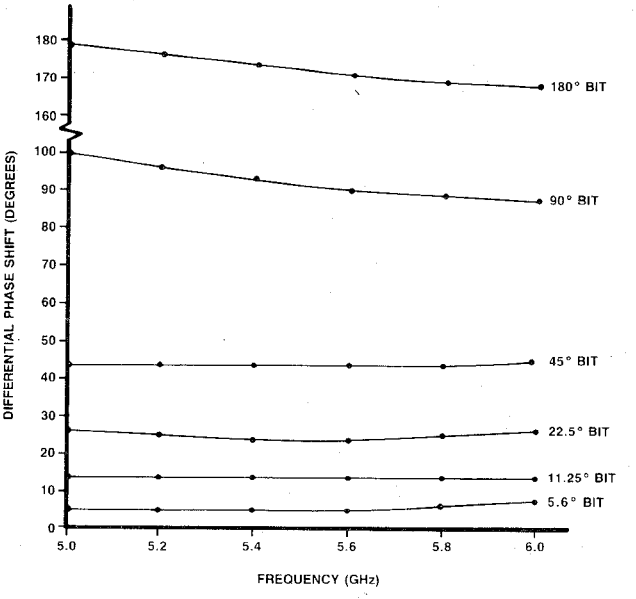

Fig. 9. Measured phase shift versus frequency for the 6-bit phase shifter.

AuGe/Ni metalization for ohmic contacts, 1-μm-long Ti/Pd/Au Schottky gates and mesa resistors. The air bridges, microstrip lines, and bonding pads are 3-μm plated gold. The wafer is lapped to its final thickness of 125 μm and diced. A photograph of the 6-bit phase shifter circuit is shown in Fig. 7.

IX. EXPERIMENTAL RESULTS

The phase shifter chips have been tested by mounting them along with 50-Ω input and output microstrip lines on a 250-μm-thick alumina substrate on a gold-plated carrier. A typical fixture mounted with APC-7 connectors and having the 6-bit phase shifter circuit is shown in Fig. 8. Various parameters of this circuit, viz., phase shift, return loss, and insertion loss measured using an HP8408A Network Analyzer, are shown in Figs. 9–11, respectively. Fig. 12 shows the variation of phase shift versus gate voltage at 5.5 GHz (the center frequency of the phase shift circuit) for the variable bit. A sixth digital bit (5.6°) may be realized by biasing the analog bit at −1.9 V.

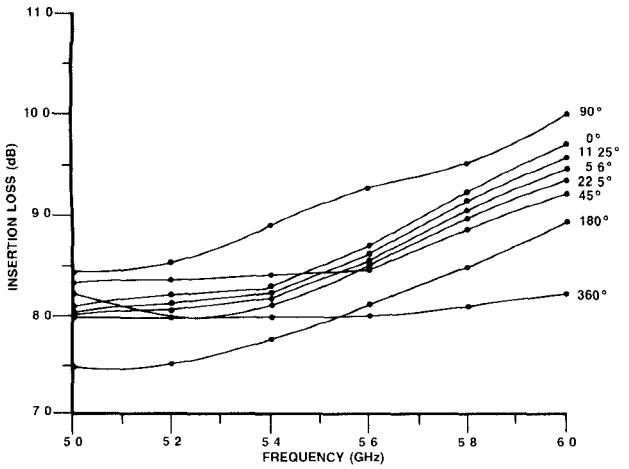

Fig. 10. Measured insertion-loss versus frequency for the 6-bit phase shifter.

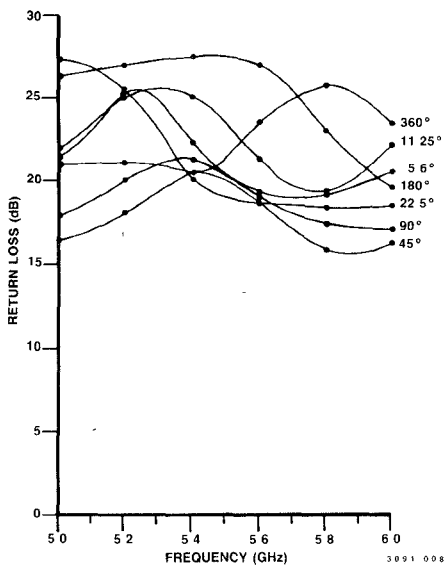

Fig. 11. Measured return-loss versus frequency for the 6-bit phase shifter.

Measured results for the first iteration 6-bit phase shifter design showed excellent conformity to the design specifications (Tables III and V) for all the bits. Table VII summarizes the test results for phase shift, return loss, and insertion loss over the 5–6-GHz frequency range. The complete chip insertion loss was measured to be 8.7 dB with a maximum loss variation of ± 1.2 dB over all phase shift values. The phase shifter characteristics were also measured for all 64 bit states. The worst-case phase error was less than $\pm 9°$, maximum insertion loss was 10 dB, and minimum return loss was 15 dB over the 5–6-GHz band. This is the best performance reported for a monolithic phase shifter of which the author's are aware [1]–[4]. Further performance improvement can be obtained by additional optimization of the line lengths between the various phase bits, and by adding an n^+ layer under the ohmic contacts to reduce FET 'on' resistance.

The performance of the circuit has also been measured against temperature. The phase variation over the 25–80°C temperature range and 5–6-GHz frequency band was less

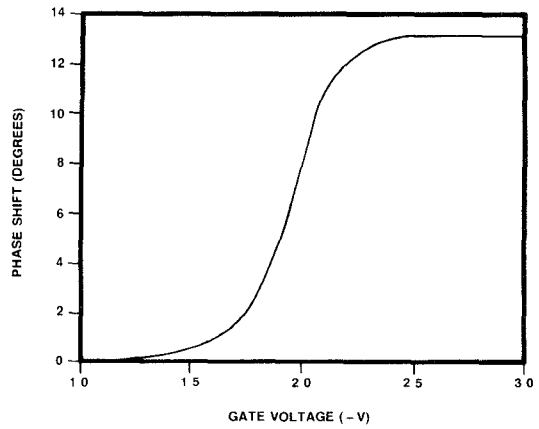

Fig. 12. Variation of phase shift as a function of gate voltage at 5.5 GHz for the variable phase bit.

TABLE VII
SUMMARY OF TEST RESULTS OVER 5–6-GHz FREQUENCY RANGE.

Bit	Phase Shift (degrees)	Return Loss (dB)	Insertion Loss Difference (dB)
11.25°	12 ± 1	>19	<.2
22.5°	23 ± 1	>18	<.5
45°	44 ± 1	>15	<.5
90°	94 ± 6	>17	<.7
180°	173 ± 6	>17	<.8
Analog	0 to 13° -1 to -3 Volts	>19	<.3

than $\pm 0.5°$, $\pm 1°$, $\pm 1°$, $\pm 2°$, and $\pm 2°$ for 11.25°, 22.5°, 45°, 90°, and 180° bits, respectively. Over the same temperature and frequency range, the insertion-loss variation was 0.6-dB maximum at minimum phase shift and 0.8-dB maximum at maximum phase shift.

X. Conclusions

A *C*-band 6-bit GaAs monolithic phase shifter having five digitally controlled bits and an analog bit for fine tuning has been successfully designed, fabricated, and tested. Excellent phase accuracy with good chip-to-chip phase tracking over 25° to 80°C has been demonstrated. These results, which are the first reported for a 6-bit monolithic phase shifter, represent a significant improvement in monolithic phase shifter performance. This excellent performance, along with small size, negligible dc power dissipation, and a few nanosecond switching times (RC constant for a 2.4-mm FET with 5-k Ω resistor is about 4 ns) make these MMIC phase shifters practical for many applications such as phased-array radars and future space-based array systems.

Acknowledgment

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In 1976, he joined ITT Gilfillan and was responsible for the development of receivers and synthesizers for radars. For the past several years, he has worked on designing the components for a phased-array radar transceiver using GaAs monolithic circuits.

His previous experience includes Sperry, where he worked in the Radar Systems Analysis Group. Later at TRW, he developed microwave hardware for space communication; and at Systron Donner Microwave, he was responsible for spectrum analyzer development.

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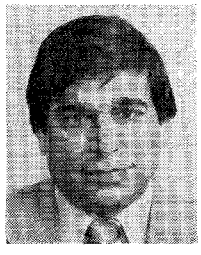

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Dr. Bahl is the author/coauthor of over 75 research papers and technical reports. He coauthored three books: *Microstrip Lines and Slotlines*, *Microstrip Antennas*, and *Millimeter Wave Engineering and Applications*.

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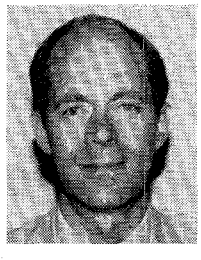

Edward L. Griffin (M'76) was born in Philadelphia, Pennsylvania, in 1947. He obtained his B.S. in Engineering Physics in 1969, his M.S. in Physics in 1971, and his Ph.D. in Solid State Physics in 1975, all from the University of Illinois.

Dr. Griffin joined the Hughes Aircraft Space and Communications Group in 1975 where he participated in the development of a wide variety of microwave components including microwave filters, and both power and low noise GaAs hybrid amplifiers. In 1982, Dr. Griffin joined the ITT GaAs Technology Center in his present capacity as manager of the design and test department.